IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/218,279, filed August 13, 2002, ~~pending,~~ now U.S. Patent 6,636,068, issued October 21, 2003, which is a continuation of application Serial No. 09/944,509, filed August 30, 2001, now U.S. Patent 6,452,415, issued September 17, 2002, which is a continuation of application Serial No. 09/083,819, filed May 22, 1998, now U.S. Patent 6,313,658, issued November 6, 2001.

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] Field of the Invention: This invention relates in general to integrated circuits (ICs) fabricated on semiconductor wafers and, more specifically, to devices and methods for isolating a short-circuited IC from other ICs on a semiconductor wafer so that, for example, probe testing may proceed on the other ICs on the wafer despite the presence of the ~~short-circuited~~ short-circuited IC.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] Therefore, there is a need in the art for a device and method for isolating a ~~short-circuited~~ short-circuited IC on a semiconductor wafer from other ICs on the wafer. Preferably, such a device and method should isolate a short-circuited IC before the IC interferes with probe testing of other ICs so the probe testing can continue uninterrupted.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] An inventive device for isolating a short-circuited integrated circuit (IC) from other ICs formed on the surface of a semiconductor wafer that are interconnected with the ~~short-circuited~~ short-circuited IC includes control circuitry within the short-circuited IC for sensing the short circuit. The control circuitry may sense the short circuit in a variety of ways, including sensing excessive current drawn by the short-circuited IC, and sensing an abnormally low or high voltage within the short-circuited IC. Switching circuitry also within the short-circuited IC

selectively isolates the short-circuited IC from the other ICs on the wafer in response to the control circuitry sensing the short circuit. As a result, if the wafer is under probe test, for example, testing can continue uninterrupted on the other ICs while the short-circuited IC is isolated.

Please replace paragraph number **[0017]** with the following rewritten paragraph:

[0017] As shown in FIG. 2, an integrated circuit (IC) 20 in accordance with the present invention includes control circuitry 22 for sensing a short in a circuit 24 internal to the IC 20 and switching circuitry 26 for isolating the internal circuit 24 from a supply voltage V_{CC} bond pad 28 on the IC 20 in response to the control circuitry 22 sensing the short. By isolating the ~~short-circuited~~ short-circuited internal circuit 24 from the supply voltage V_{CC} bond pad 28, the present invention can prevent the short from "tripping" probe test equipment (not shown) supplying the supply voltage V_{CC} to a semiconductor wafer (not shown) during probe testing of the wafer.

Please replace paragraph number **[0025]** with the following rewritten paragraph:

[0025] As shown in FIG. 6 in another alternative embodiment of the present invention, an IC 80 includes control circuitry 82 for sensing a short in a circuit 84 internal to the IC 80 and switching circuitry 86 for isolating the internal circuit 84 from a supply voltage V_{CC} bond pad 88 on the IC 80 in response to the control circuitry 82 sensing the short. By isolating the ~~short-circuited~~ short-circuited internal circuit 84 from the supply voltage V_{CC} bond pad 88, the present invention can prevent the short from "tripping" probe test equipment (not shown) supplying the supply voltage V_{CC} to a semiconductor wafer (not shown) during probe testing of the wafer.

Please replace paragraph number **[0028]** with the following rewritten paragraph:

[0028] When a short circuit (e.g., a short circuit to ground) does exist in the internal circuit 84, the internal circuit 84 rapidly draws excessive current I through the resistor 104, causing the voltage drop V across the resistor 104 to exceed the threshold voltage $|V_T|$ of the sensing PMOS transistor 106. As a result, the sensing PMOS transistor 106 turns on, thereby

applying the supply voltage V_{CC} at the base 96 of the switching BJT 98 and raising the voltage applied at the input to the inverter 100. The rising voltage at the input of the inverter 100 causes the inverter 100 to output a low voltage at the gate of the hysteresis PMOS transistor 102, thereby turning the hysteresis PMOS transistor 102 on and reinforcing application of the supply voltage V_{CC} at the base 96 of the switching BJT 98. This causes the switching BJT 98 to turn off, thereby interrupting the excessive current flow I and isolating the short-circuited internal circuit 84 from the bond pad 88.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] It should be understood that the micro-relay may be created using silicon ~~micro-machining~~ micro-machining techniques, and may comprise a capacitively or inductively controlled relay.